An Application-Specific DSP for Portable Applications

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This paper describes the features, the architecture and a few applications of the PINE™ DSP core. PINE is a 16-bit Digital Signal Processor designed for portable telecommunications and consumer electronics products requiring smart power management. It enables low-cost, low-power DSP processing with several levels of modularity in the RAM, ROM and I/O, permitting efficient DSP-based ASIC development. PINE's modular design approach allows the same DSP core to be used for various applications.

1. INTRODUCTION

In recent years we have seen a proliferation of compact, powerful consumer electronic devices, including CD players, minidisk players, personal digital assistants (PDAs) and cellular telephone products. These devices push the boundaries of both performance and miniaturization. Combined with the cost constraints of the consumer markets, these devices require cost-efficient, performance-optimized DSP hardware and sophisticated, application-tuned DSP algorithms.

PINE™ is a 16-bit Digital Signal Processor designed for portable telecommunications and consumer electronics products requiring smart power management. It enables low-cost, low-power DSP processing with several levels of modularity in the RAM, ROM and I/O, permitting efficient DSP-based ASIC development.

It's design was application-driven, based on extensive analysis of the target applications and the instructions and architectural features essential to those applications. A detailed static and dynamic statistical analysis of the instructions usage in the applications have been performed. The instruction set was defined based on this analysis and was also enhanced with instructions to support microcontroller functions.

PINE's modular design approach allows the same DSP core to be used for various applications simply by adding on-chip memory, peripherals and custom logic. To

quickly move from concept to silicon requires the right development tools, especially software development tools, which support this architectural approach.

2. DSP CORE KEY FEATURES

The following list describes the main features of the PINE DSP core.

Technology

* Double metal CMOS technology
* 25 ns cycle time @ 5V
* Power Management:
  - fully static design
  - wide operating voltage range 3-5.5V
  - low power dissipation
  - SLOW mode
  - STOP mode

Architecture

* 16-bit fixed-point DSP core with a high level of modularity:
  - expandable Data RAM/ROM
  - expandable Program ROM
  - up to 8 user-defined registers
  - up to 16 levels of stack
* 16x16-bit multiplier; single cycle multiply-accumulate instructions
* 36-bit ALU; two 36-bit accumulators
* Six general-purpose, 16-bit pointer-registers with two dedicated address arithmetic units for data memory indirect addressing, circular buffering, loop counters, and program memory indirect addressing.
* Zero Overhead Looping, REPEAT and BLOCK-REPEAT instructions
* Automatic saturation mode
* Divide and Normalize step support
* Advanced, Windows™-based Development Tools

3. ARCHITECTURE

A block diagram of the DSP core is shown in Figure 1. The main blocks of the DSP core are a Computation Unit (CU), which includes ALU, multiplier and accumulators, a Data Address Arithmetic Unit (DAAU), and a Program Control Unit (PCU). All other peripheral blocks including program and data memory, which are application-specific, are defined as part of the user-specific logic, implemented around the core on the same silicon die.

Data is transferred on the following 16-bit buses: a bidirectional X Data Bus (XDB), and two unidirectional buses - the Y Data Bus (YDB) and the Program Data bus (PDB). The XDB is the main data bus, where most of the data transfers occur. Instruction word fetches take place in parallel over the PDB. The bus structure can transfer up to two 16-bit words in the same instruction cycle.

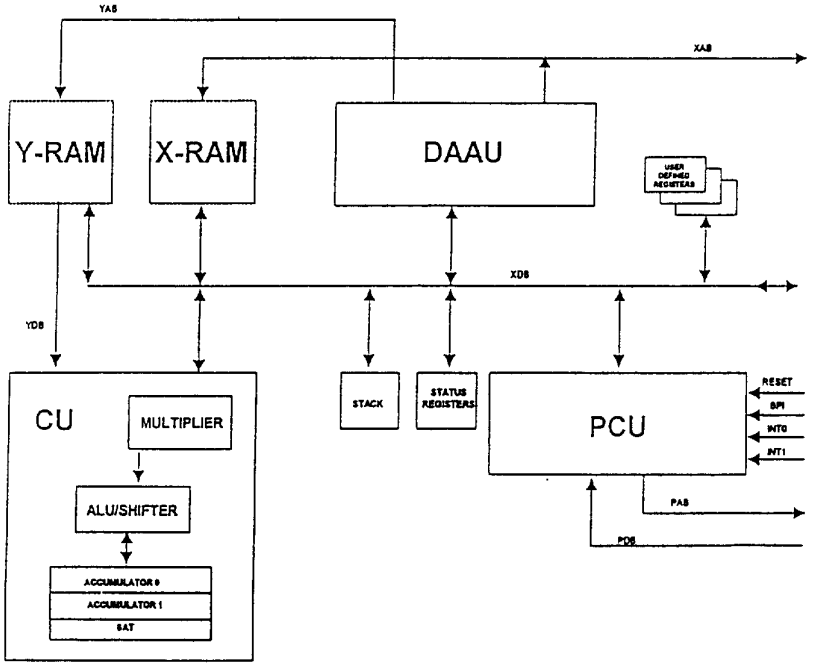

Figure 1. PINE Block Diagram

The X Address Bus (XAB) and the Y Address Bus (YAB) drive the addresses for XRAM and YRAM. The Program Address Bus (PAB) drives the program memory addresses.

Computation Unit

The computation unit is the heart of the DSP. It contains the multiplier, the ALU, and the two accumulators.

The multiplier unit consists of a 16x16 bit single-cycle, non-pipelined multiplier, two 16-bit input registers (X and Y), a 32-bit output register (P), and an output shifter. Together with the Data ALU, PINE can perform a single-cycle Multiply-Accumulate (MAC) instruction. The P register is updated only after a multiply instruction and not after a change in the X and/or Y registers.

The P register is sign-extended into 36 bits and then shifted. The output shifter is capable of shifting data from the P register into the ALU.

The Data ALU performs all arithmetic, logical and shifting operations on data operands. The Data ALU consists of a 36-bit, single-cycle, non-pipelined ALU unit, two 36-bit accumulator registers (A0 and A1), and a saturation unit.

The ALU can perform a positive or negative accumulate, add, subtract, compare, shift, logical, and several other operations, most of them in one instruction cycle. It uses a 2's complement arithmetic.

Each accumulator is organized as two regular 16-bit registers (A0H, A0L, A1H and A1L) and a 4-bit extension nibble (A0E and A1E). The extension nibbles A0E and A1E offer protection against 32-bit overflow. Saturation arithmetic is provided to selectively limit overflow when reading A0 or A1 from the A0H or A1H portion of an accumulator to the A0E or A1E portion respectively. The ALU unit supports normalization, division and rounding.

Data Address Arithmetic Unit

The Data Address Arithmetic Unit (DAAU) performs all address calculations necessary to address data operands in data and program memories. In addition, it supports loop counter operations. This unit operates in parallel with other core resources to minimize address generation overhead. The DAAU can implement

linear and modulo arithmetic. The DAAU contains six address registers for indirect addressing, and two configuration registers for modulo and increment/decrement step control. The registers are divided into two groups for simultaneous addressing over XAB and YAB (or PAB).

The DAAU can generate two addresses every instruction cycle which can be post-modified by two modifiers: linear and modulo. The address modifiers allow the creation of data structures in memory for circular buffers, delay lines, FIFOs, software stacks, etc.

The modulo modifier implemented in PINE is a simplified mechanism especially designed to achieve small silicon area [1]. It requires that the modulo size should be an integer multiple of the step size. This restriction has a minor effect on algorithms' implementation, but has a major effect on hardware complexity.

Program Control Unit

The Program Control Unit (PCU) performs instruction fetch, instruction decoding, exception handling, and wait state support. In addition, it supports a mechanism for internal PROM protection.

The PCU generates the next address to the program memory and controls hardware loops. It contains the Repeat/Block-Repeat unit, and two 16-bit registers: the Program Counter and the Loop Counter.

The Repeat/Block-Repeat unit performs hardware-loop calculations and control, with no overhead other than the one-time execution of set-up instructions REP and BKREP. It consists of two 16-bit dedicated registers for start and end addresses of the block-repeat, and two 8-bit repeat and block-repeat counters.

The program controller implements a three-level pipeline architecture. In the operation of the pipeline, concurrent fetch, operand fetch and execution occur. This allows instruction execution to overlap. Thus, the effective execution time for most instructions is one cycle. Each pipeline stage is completed before its result is needed by the next instruction. The pipeline is an "interlocking" pipeline, transparent to the user, which simplifies programming.

Memory Organization

Two independent 64K word memory spaces are available: the data space (XRAM and YRAM) and the program space (PROM).

The data space of PINE has a unique and novel structure [2]. It is divided into an X data space for the XRAM, and a Y data space for the YRAM, both residing in the 64K word data memory space. The XRAM space has an internal space (on-core data RAM or ROM) of 1K word, and an external off-core space of 62K. The YRAM space is 1K word internal only (RAM or ROM). The above data space partition allows modular expansion of the internal XRAM and YRAM, and at the same time enables the two RAMs to be viewed as single **continuous** data RAM. This data structure virtually emulates a dual-port RAM but consumes about 70% of its silicon area.

PINE core peripherals are memory mapped I/O into the data space and are depending on the Application Specific DSP (ASDSP) configuration.

The program memory PROM can be implemented as internal and/or external memory up to a total of 64K words.

The PINE DSP core supports eight optional user-definable registers, which can be located off-core. This enables expansion of the core. These registers appear in the data register fields of all relevant instructions. With these registers, external computation units can be loaded with data and read at the end of the computation directly into internal registers in a single cycle. Operations such as parity calculation, location of first-1-bit in a word, special shifts, and min/max/mid value can be easily performed in parallel in a few cycles with the PINE core.

Power Management

PINE has two power save operation modes, the slow and stop modes.

SLOW mode: The PINE clock can be slowed down by writing a 4-bit value to a special memory-mapped register located external to the core. The clock division factor can be 1, 2,..., 16. The core power dissipation is reduced as follows:

3+22/N mA for 5V operation, and
1.3+9.7/N mA for 3.3V operation,

where N is the clock division factor.

STOP mode: Since the PINE core VLSI design is fully static, the clock can be stopped by setting a special bit. The reset signal will reactivate the core. The RAM content and all registers which are not defined as being affected by the reset will remain unaffected.

Instruction Set

PINE's 16-bit instruction encoding has been optimized to support the highest parallelism allowed by the architecture. Several of the most common DSP benchmarks are shown in Table 1. The instructions fall into 6 groups: arithmetic and logical, multiply and multiply-accumulate, move, branch and call, loop and control. The instruction set was designed to support both DSP requirements as well as general purpose control functions.

PINE DSP Benchmark	Execution Time
N taps FIR filter	N x 25ns
N taps LMS	4N x 25ns
N taps complex FIR filter	4N x 25ns
N Cascaded IIR Biquads	5N x 25ns

Table 1. PINE Benchmarks

4. APPLICATIONS

The PINE architecture, which provides powerful DSP while keeping low power dissipation, is attractive to many portable applications such as mobile computing, cellular phones, wireless PBX, wireless data, Personal Digital Assistants (PDAs) and personal audio. Following are two applications which benefit from this architecture.

Cellular Communications

The new digital cellular standards call for state-of-the-art speech coding, channel coding and modem techniques needed to implement speech coders such as VSELP or half-rate GSM, channel coders and modems such as DQPSK. The speech and

channel coders can be realized most efficiently with DSP techniques. Similarly, the modulation/demodulation schemes set forth in the various standards, are best implemented with DSP-based solutions. Integrating all these functions in a single application specific DSP, tightly tailored to meet the customer requirements will provide the best solution at lowest possible cost. Additionally, the reduced battery power requirements will extend battery life, or, alternatively, permit the batteries to be smaller. Other capabilities, soon to appear on the market, including acoustical echo cancellation, voice-activated dialing and noise reduction are all DSP-based and can be easily integrated either by adding more software (more program memory) or adding more on-chip peripherals to support these functions.

Personal Digital Assistants

The market for handheld computers, sometimes called Personal Digital Assistants, is expected to grow from 2 million units to over 10 million units annually by 1995. These mobile, handheld information management devices offer multiple interfaces such as pen, voice, mouse and keyboard. By incorporating wireless communication technologies such as cellular or data packet radio, they can allow the user to access information services and send and receive email, faxes and voice messages.

Because these new systems push the absolute limits of performance, integration and low power consumption, they present a formidable challenge to IC suppliers and systems designers alike. The DSP processing requirements for such advanced capabilities as speech and handwriting recognition on top of modem and wireless capabilities, are substantial and require a highly optimized DSP-based solution. An ASDSP solution is essential to achieve the high degree of integration required by these "pico-computers."

5. SUMMARY

Faced with escalating demands for high performance, high functionality, miniaturization and smart power utilization, designers are becoming increasingly aware of the limitations of general-purpose DSP architectures. PINE was developed specifically to fill this growing need. Its highly optimized, modular architecture, combined with a complete set of development tools, will permit designers not only to achieve their performance, size and power goals, but to meet the ever shrinking windows of opportunity in today's consumer electronics markets.

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